## ***REMARKS***

Applicants thank the Examiner for the thorough examination of the application. Claims 1-18 are pending. Claims 1, 2, and 4 are amended. Claims 1 and 10 are independent. Reconsideration of the present application, as amended, is respectfully requested.

### ***Drawings***

The drawings are objected to as being incomplete. Specifically, the Examiner contends that FIGS. 6 and 7 do not adequately illustrate the "hole" and related "protrusion." Included with the accompanying Letter to the Official Draftsperson are proposed changes to FIGS. 1, 4, 6, and 7. Upon approval, the proposed changes will be incorporated into the formal drawings. In view of the proposed changes, withdrawal of the objection to the drawings is respectfully requested.

### ***Claim for Priority***

The Examiner has recognized Applicants' claim for foreign priority and receipt of the certified copy of the priority document. No further action is required at this time.

***Rejection under 35 U.S.C. §112, second paragraph***

Claim 4 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 4 is amended to recite that the gate dummy pattern includes a *recess* connected to the gate line and formed to permit a repair. According, withdrawal of the rejection of claim 4 is respectfully requested.

***Rejections under 35 U.S.C. §102(e)/§103(a)***

Claims 1, 2, and 5 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,429,909 to Kim et al. Claims 3 and 4 are rejected 35 U.S.C. §103(a) as being unpatentable over Kim et al. Claims 3, 4, 6, and 7 are rejected as being unpatentable over Kim et al. in view of U.S. Patent No. 6,313,889 to Song et al. These rejections are respectfully traversed.

While not conceding the appropriateness of the rejection, but merely to advance prosecution of the instant application, claim 1 is amended to recite a thin film transistor substrate in a liquid crystal display having a combination of elements, including a gate dummy pattern which extends vertically from the gate line and overlaps with the data line and the pixel electrode, the gate dummy pattern being integrated with the data line.

It is respectfully submitted that the combination of elements set forth in independent claim 1 is not anticipated or rendered obvious by the art of record, including Kim et al. and Song et al.

In an LCD in which a pixel electrode and a gate dummy pattern are overlapped to achieve a high aperture ratio LCD, it is generally difficult to ensure a process margin for repairing disconnection defects of data lines. In the present invention, the recess is formed to ensure a process margin.

More specifically, the recess is cut during disconnection of a data line, and the disconnected data line and the gate dummy pattern are connected to each other using a laser welding technique, thereby repairing the disconnection of the data line. A protrusion of the data line is formed to cover the recess part for shutting off a light leaked from the recess part after cutting the recess.

The present invention has features of a gate dummy pattern which is formed when forming a gate line and a gate electrode, upon disconnection of the data line, the gate dummy pattern is separated from the gate line and connected to the disconnected data line for repair.

The present invention also is characterized in that in a normal state, when the disconnection of the data line has not occurred, the gate dummy pattern is used to secure a large storage capacitance,

and to shut off leakage. Therefore, in the present invention, the gate dummy pattern is insulated with the data line.

In contrast to the present invention, Kim et al. merely discloses an LCD including a gate line 100, repair lines 110 and 120, a gate line 400, a gate-insulating film 200, a passivation film 500, and a pixel 600, as shown in FIGS. 6, 7, and 13. Contact holes C5-C8 are formed in the gate-insulating film 200. However, Kim et al. does not teach or suggest a gate dummy pattern formed in such a manner as to be extended in a vertical direction from the gate line and to overlap with data line and the pixel electrode, the gate dummy pattern being insulated with the data lines, as recited in claim 1.

In rejecting claims 3, 4, 6, and 7, the Office Action relies on Song et al. for teachings of the use of a redundant pattern as a redundancy electrode, a substrate wherein the left and right auxiliary gate lines includes a disconnect, and a storage capacitor defined by a horizontal overlapping part between a gate line and a pixel electrode. However, Song et al. does not teach or suggest the above-cited limitation of claim 1 and, therefore, fails to cure the deficiencies of Kim et al.

Added claims 10-18 recite additional aspects of the present invention and are fully supported by the specification. Applicants

respectfully submit that claims 10-18 are not anticipated or obvious over the cited art.

In view of the foregoing, it is respectfully submitted that the art of record, including Kim et al. and Song et al., fails to teach or suggest the combinations of elements set forth in claims 1 and 10-18. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §102(e) and §103(a) are respectfully requested. It is believed that claims 1 and 10-18 are allowable. Since the remaining claims depend from these allowable claim 1, they are also allowable for at least the above reasons, as well as for the additional limitations provided thereby. Thus, all claims are allowable.

***Conclusion***

Since the remaining patents cited by the Examiner have not been utilized to reject claims, but merely to show the state of the art, no comment need be made with respect thereto.

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

However, if there are any outstanding issues, the Examiner is invited to telephone Sam Bhattacharya (Reg. No. 48,107) at (703) 205-8000 in an effort to expedite prosecution.

Pursuant to 37 C.F.R. §§1.17 and 1.136(a), Applicants hereby request a one-month extension of time in which to file this reply. A check for the required fee of $110 is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or to credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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***MARKED-UP COPY OF AMENDMENTS***

***In the Abstract***:

Please **amend the Abstract** as follows:

**Abstract**

A liquid crystal display [with] has a gate line structure [capable of] for serving as a storage electrode and a black matrix and performing a repair function [is disclosed]. In the liquid crystal display, a gate dummy pattern is formed in such a manner to be extended in the vertical direction from the gate line and to overlap with the data line and the pixel electrode. [Accordingly, the] The gate dummy pattern [branched] branches from the gate line [and overlapping], overlaps the edge of a pixel, serves a storage electrode and a black matrix, and permits [a] repair upon [break] breakage of a data line.

***In the Specification***:

Please **amend the paragraph beginning on page 1, line 32,** and **ending on page 3, line 19,** to divide the text into three paragraphs as follows:

**[**Referring to**]** Fig. 1**[**, there is shown**]** shows a thin film transistor substrate **[**of the**]** for a conventional liquid crystal display (LCD). The LCD includes thin film transistors 6 positioned at intersections between data lines 2 and gate lines 4, and pixel electrodes 14 connected to drain electrodes 12 of the thin film transistors 6. The thin film transistor 6 is provided at an intersection between the data line 2 and the gate line 4. The thin film transistor 6 has a gate electrode 10 connected to the gate line 4, a source electrode 8 connected to the data line 2, and a drain electrode 12 connected, via a first contact hole 16, to the pixel electrode 14.

The thin film transistor 6 further includes a semiconductor layer (not shown) for providing a conductive channel between the source electrode 8 and the drain electrode 12 by a gate voltage applied to the gate electrode 10. **[**Such a**]** The thin film transistor 6 responds to a gate signal from the gate line 4 to selectively apply a data signal from the data line 2 to the pixel

electrode 14. The pixel electrode 14 is positioned at a cell area divided by the data line 2 and the gate line 4, and is made from [a] an indium tin oxide (ITO) material having [a] high light-transmissivity. The pixel electrode 14 generates a potential difference from a common transparent electrode (not shown) provided at [the] an upper glass substrate by a data signal applied via the first contact hole 16. By virtue of this potential difference, a liquid crystal positioned between the thin film transistor substrate and the upper substrate is rotated [by] according to its dielectric anisotropic property and a light applied, via the pixel electrode 14, from a light source is transmitted into the upper glass substrate.

A storage capacitor 18 provided between the pixel electrode 14 and the gate line 4 at the previous stage plays a role [to prevent a] in preventing voltage variation in the pixel electrode 14 by charging a voltage in a period at which a gate high voltage is applied to the previous-stage gate line 4 and discharging the charged voltage in a period at which a data signal is applied to the pixel electrode 14. Since, as stated, the storage capacitor 18 aims at maintaining a stable pixel voltage [as mentioned above], it must have a high capacitance value. To this end, the storage capacitor 18 has a structure as shown in Fig. 2.

In Fig. 2, the storage capacitor 18 is defined by a storage electrode 20 electrically connected, via a second contact hole 22 formed in a protective film 28, to the pixel electrode 14 and a gate electrode 4 having on a gate insulating layer 26 therebetween. The storage electrode 20 is formed on the gate insulating layer 26 upon formation of the data line 2 and the source/drain [electrode] electrodes 8 and 12. As a liquid crystal panel goes into a larger dimension, [a] the capacitance value of the storage capacitor 18 must be [more enlarged] increased. However, the above-mentioned LCD structure [has a limit in enlarging a] is limited in its ability to enlarge the capacitance of the storage capacitor 18.

Please **amend the paragraph beginning on page 3, line 21**, and **ending on page 4, line 1**, as follows:

The protective film 28 of the thin film transistor substrate is usually made from an inorganic material having a dielectric constant such $SiN_X$ or $SiO_X$ . The pixel electrode 14 and the data line 2 having such an inorganic protective film therebetween maintain a certain horizontal distance d (e.g., 3 to 5μm), as shown in Fig. 3, so as to minimize [a] any coupling effect caused by a parasitic capacitor. In this case, in order to shut off [a] light [leaked] leaking through the space between the data line 2 and the

pixel electrode 14, a black matrix formed on the upper substrate has a width [enough] sufficient to cover a portion of the pixel electrode 14 positioned at each side of the data line 2. As a result, [an] the aperture ratio of the liquid crystal cell is inevitably reduced.

Please **amend the paragraph beginning on page 4, line 9**, as follows:

A further object of the present invention is to provide a liquid crystal display that is capable of reducing [a] the width of a black matrix to increase an aperture ratio, as well as [performing a repair function] to allow for repairs upon [break] breakage of a data line.

Please **amend the paragraph beginning on page 4, line 14**, as follows:

In order to achieve these and other objects of the invention, a thin film transistor substrate in a liquid crystal display according to the present invention includes a gate dummy pattern formed [in such a manner] so as to [be extended in the vertical direction] extend vertically from the gate line and to overlap with the data line and the pixel electrode.

Please **amend the paragraph beginning on page 4, line 27,** as follows:

Fig. 1 is a plan view showing a structure of a thin film transistor substrate in a [convention] conventional liquid crystal display;

Please **amend the paragraph beginning on page 4, line 30,** as follows:

Fig. 2 is a [section] sectional view of a portion of the storage capacitor [part] taken along [the] line A-A' [line] in Fig. 1;

Please **amend the paragraph beginning on page 4, line 32,** as follows:

Fig. 3 is a [section] sectional view of a portion of the data line [part] taken along [the] line B-B' [line] in Fig. 1;

Please **amend the paragraph beginning on page 5, line 4,** as follows:

Fig. 5 is a [section] sectional view of a portion of the data line [part] taken along [the] line A-A' line in Fig. 4;

Please **amend the paragraph beginning on page 5, line 7,** and **ending on page 7, line 21,** to divide the text into six paragraphs as follows:

Referring to Fig. 4, there is shown a thin film transistor substrate in a liquid crystal display (LCD) according to a first embodiment of the present invention. The LCD includes thin film transistors 6 positioned at intersections between data lines 2 and gate lines 4, pixel electrodes 14 connected to drain electrodes 12 of the thin film transistors 6, and gate dummy patterns 30 overlapping **[**with**]** the data lines 2 and the pixel electrodes 14 adjacent to the data lines 2. The thin film transistor 6 has a gate electrode 10 connected to the gate line 4, a source electrode 8 connected to the data line 2, a drain electrode 12 connected, via a first contact hole 16, to the pixel electrode 14, and a semiconductor layer (not shown) for providing a conductive channel between the source electrode 8 and the drain electrode 12 by virtue of a gate voltage applied to the gate electrode 10.

Such a thin film transistor 6 responds to a gate signal from the gate line 4 to selectively apply a data signal from the data line 2 to the pixel electrode 14. The pixel electrode 14 generates a potential difference from a common transparent electrode (not

shown) provided at [the] an upper glass substrate by a data signal applied via the first contact hole 16. By virtue of this potential difference, a liquid crystal positioned between the thin film transistor substrate and the upper substrate is rotated [by] according to its dielectric anisotropic property and a light applied, via the pixel electrode 14, from a light source is transmitted into the upper glass substrate.

A storage capacitor 18 provided between the pixel electrode 14 and the gate line 4 at the previous stage plays a role [to prevent a] in preventing voltage variation in the pixel electrode 14 by charging a voltage in a period at which a gate high voltage is applied to the previous-stage gate line 4 and discharging the charged voltage in a period at which a data signal is applied to the pixel electrode 14. The storage capacitor 18 is defined by a storage electrode 20 electrically connected, via a second contact hole 22 formed in a protective film 28, to the pixel electrode 14 and a gate electrode 4 having a gate insulating layer 26 therebetween. The storage electrode 20 is formed on the gate insulating layer 26 upon formation of the data line 2 and the source/drain [electrode] electrodes 8 and 12.

The gate dummy pattern 30 overlaps with the data line 2 and the adjacent pixel electrode 14 to serve as a black matrix, as well

as to [perform a repair function] allow for repairs upon [break] breakage of the data line. For instance, the gate dummy pattern 30 is electrically connected to a broken data line 2 [by] using a laser welding technique upon [break] breakage of the data line 2 to permit a repair. Also, the gate dummy pattern 30 is positioned [in such a manner] so as to overlap, by about 0.5 to 1μm, [with] the data line 2 and the pixel electrode 14, thereby serving as a black matrix [for shutting] to shut off [a] light [leaked] leaking between the data line 2 and the pixel electrode 14.

When the gate dummy pattern 30 is used as a black matrix [as mentioned above], an area overlapping [with] the pixel electrode 14 can be [more] further reduced in comparison to [the] conventional black [matrix] matrices to [expect] provide an increase in the aperture ratio [increase] of about 5 to 6%. To this end, the gate pattern 30 is formed on a lower substrate 24 with [having] the gate insulating layer 26 at each side of the data line 2, as shown in Fig. 5. [This] The gate dummy pattern is made from the same material (e.g., Al, Mo, Ti, W, Cr or Cu) as the gate line and the gate electrode. [Such a] The above-described gate dummy pattern 30 may be provided at both sides of the data line 2 or at one side of the data line 2.

If the gate dummy pattern 30 is electrically connected to the gate line 4, [then] it can be used as a storage electrode forming, along with the pixel electrode 14, the storage capacitor [along with the pixel electrode 14], overlapped with having the gate insulating layer 26 and the protective film 28 therebetween. In this case, [a] the capacitance value of the storage capacitor caused by the gate dummy pattern 30 is added to the conventional storage capacitor 18, so that [a] the voltage of the pixel electrode 14 can be maintained at a more stable state.

Please **amend the paragraph beginning on page 7, line 23**, and **ending on page 8, line 31**, to divide the text into multiple paragraphs as follows:

[Referring to] Fig. 6[, there is shown] shows a thin film transistor substrate in a liquid crystal display (LCD) according to a second embodiment of the present invention. The thin film transistor substrate of Fig. 6 has the same elements as that of Fig. 4, except that [a] the gate dummy pattern 32 is electrically connected to [a] the gate line 4. The gate dummy pattern 32 is extended from the gate line 4 into [the] a lower portion thereof [in such a manner] so as to overlap [with a] the data line 2 and [a] the pixel electrode 14 at each side of the data line 2. [Such

a] In this embodiment, the gate dummy pattern 32, along with the pixel electrode 14, defines a second storage capacitor [along with the pixel electrode 14] overlapped with [having] a gate insulating layer and a protective film. As a result, [a] the capacitance value of the second storage capacitor caused by the gate dummy pattern 32 is added to the [existent] existing storage capacitor, that is, the first storage capacitor 18, so that [a] the voltage at the pixel electrode 14 [can maintain] is more stable [state]. In addition, the gate dummy pattern 32 [permits a repair] allows for repairs upon [break] breakage of the data line 2.

In order to [provide a repair] effect repairs of the data line 2, it must be opened to the gate line 4. However, when the gate line 4 and the gate dummy pattern 32 [is] are cut by means of a laser, the data line 2 overlapping with the gate dummy pattern 32 is also [is] cut away. In order to prevent [a] damage [of] to the data line 2, a [hole] recess 32a is provided at a cutting part for breaking the gate line 4 and the gate dummy pattern 32 [in such a manner] so as to not [be not overlapped with] overlap the data line 2, as shown in Fig. 6. Accordingly, [upon break of] if the data line 2 breaks, [a repair] repairs can be [performed] effected by cutting the [hole] recess 32a provided in the gate dummy pattern 32 using a laser to electrically [break] separate the gate line 4

from the gate dummy pattern 32 and thereafter electrically connecting the broken data line 2 to the gate dummy pattern 32 [using the] by laser welding [technique]. [Also, the] The gate dummy pattern 32 is positioned [in such a manner] so as to overlap, by about 0.5 to [1μm, with] 1 μm, the data line 2 and the pixel electrode 14, thereby serving as a black matrix [for shutting] shut off a light [leaked] leaking between the data line 2 and the pixel electrode 14. When the gate dummy pattern 32 is used as a black matrix as [mentioned] described above, [an] the area overlapping [with] the pixel electrode 14 can be [more] further reduced in comparison to [the] conventional black [matrix] matrices to [expect] provide an aperture ratio increase of about 5 to 6%.

Please **amend the paragraph beginning on page 8, line 32**, and **ending on page 10, line 23**, as follows:

Referring to Fig. 7, there is shown a thin film transistor substrate in a liquid crystal display (LCD) according to a third embodiment of the present invention. The thin film transistor substrate of Fig. 7 has the same elements as that of Fig. 4, except that a protrusion 2a is provided at [a] the data line 2 so as to shut off [a] any light [leaked] leaking between [a] the gate line 4 and [a] the gate dummy pattern 30. The gate dummy pattern 30

formed at the same layer as the gate line 4 overlaps with a data line 2 and a pixel electrode 14 at each side of the data line 2 to serve as a black matrix for shutting off a light leaked between the data line 2 and the pixel electrode 14. In this case, in order to prevent a light from being leaked through a spaced area 34 between the gate line 4 and the gate dummy pattern 30, the data line 2 further includes a protrusion 2a overlapping with the gate line 4 and the gate dummy pattern 30. When the gate dummy pattern 30 and the protrusion 2a of the data line 2 are used as a black matrix as mentioned above, an area overlapping with the pixel electrode 14 can be more reduced in comparison to the conventional black matrix to [expect] provide an aperture ratio increase of about 5 to 6%. Also, the gate dummy pattern 30 permits a repair upon break of the data line 2. More specifically, the gate dummy pattern 30 is electrically connected to a broken data line 2 by the laser welding technique, etc. upon break of the data line 2 to permit a repair.

If the gate dummy pattern 30 is electrically connected to the gate line 4, then it can be used as a storage electrode forming the storage capacitor along with the pixel electrode 14 overlapped with having the gate insulating layer 26 and the protective film 28 therebetween. In this case, a capacitance value of the storage capacitor caused by the gate dummy pattern 30 is added to the

conventional storage capacitor 18, so that a voltage of the pixel electrode 14 can be maintained at more stable state.

Please **amend the paragraph beginning on page 10, line 3**, as follows:

As described above, according to the present invention, the gate dummy pattern branched from the gate line and overlapping with the edge of the pixel serves as a storage electrode to increase a storage capacitance value. Accordingly, since a storage capacitance value increased by virtue of the gate dummy pattern compensates for an average maintenance voltage Vrms between the pixels generated by a characteristic difference between the thin film transistors caused by a misalignment of the line patterns in the course of a process to improve a picture quality, the present LCD is adaptive for a technique of fabricating a large-dimension LCD. Furthermore, according to the present invention, the gate dummy pattern branched from the gate line and overlapping with the edge of the pixel serves as a black matrix to **[**more**]** <u>further</u> increase an aperture ratio in comparison to a case where the conventional black matrix is used. In addition, the gate dummy pattern branched from the gate line and overlapping with the edge

of the pixel is used to permit a repair upon break of the data line, so that an effect of a throughput improvement can be obtain.

***In the Claims:***

Please **amend claims 1, 2, and 4** as follows:

**1.** (Amended) A thin film transistor substrate in a liquid crystal display provided with a data **[**lines**]** line for applying a data **[**signals**]** signal, a gate line for applying a gate signal, and a pixel electrode for driving a liquid crystal cell, said substrate comprising:

a gate dummy pattern formed **[**in such a manner**]** so as to **[**be extended in the vertical direction**]** extend vertically from the gate line and to overlap with the data line and the pixel electrode, the gate dummy pattern being integrated with the data line.

**2.** (Amended) The thin film transistor substrate according to claim **1**, wherein the gate dummy pattern is formed in such a manner to overlap with one side **[**or both sides**]** of the data line and the edge of the pixel electrode adjacent thereto.

**4.** (Amended) The thin film transistor substrate according to claim **3**, wherein the gate dummy pattern includes a **[**hole**]** recess connected to the gate line and formed to permit a repair.

***CLAIMS 8-18 ARE ADDED.***